AMENDMENTS TO THE CLAIMS

The following listing of claims will replace all prior versions, and listings, of claims in this application.

1. (Original) A delay-locked loop (DLL), comprising:

a level selector, which receives an external clock signal and directly outputs the external clock signal, or changes a level of the external clock signal and outputs a changed external clock signal, in response to a control signal;

a control signal generator which generates the control signal; and

an internal clock signal generator, which receives an output signal of the level selector and the external clock signal, and generates an internal clock signal synchronized to a phase of the output signal of the level selector.

2. (Original) The DLL of claim 1, wherein the level selector comprises:

a selection controller, which directly applies the external clock signal to the internal clock signal generator or outputs the external clock signal as a level control signal in response to the control signal; and

a clock buffer unit, which generates the changed external clock signal in response to the level control signal.

3. (Original) The DLL of claim 2, wherein the selection controller comprises:

a first transmission gate, which directly applies the external clock signal to the internal clock signal generator, in response to a first level of the control signal;

a second transmission gate, which outputs the external clock signal as the level control signal, in response to a second level of the control signal; and

an inverter, which inverts a logic level of the control signal and applies the inverted control signal to the first and the second transmission gates.

4. (Original) The DLL of claim 2, wherein the clock buffer unit amplifies the level of the level control signal to a complementary metal oxide semiconductor (CMOS) level.

5. (Original) The DLL of claim 1, wherein the control signal generator generates the control signal, in response to command signals.

6. (Original) The DLL of claim 1, wherein the control signal is a mode register set (MRS) signal.

7. (Original) The DLL of claim 1, wherein the control signal generator comprises:

a first bonding pad;

a second bonding pad; and

a third bonding pad, which is connected to the first bonding pad or the second bonding pad using a bonding wire, and generates the control signal.

8. (Original) The DLL of claim 1, wherein the control signal generator comprises:

a first transistor;

a second transistor;

a third transistor;

a first inverter; and

a second inverter, which inverts an output signal of a second node and outputs the inverted output signal as the control signal.

9. (Original) The DLL of claim 8, wherein the fuse is a laser fuse.

10. (Original) The DLL of claim 8, wherein the power-up signal is generated with a second level during a time period, and generated with a first level after the time period.

11. (Original) The DLL of claim 1, wherein the external clock signal has a Transistor-Transistor Logic (TTL) level.

12. (Currently Amended) The DLL of claim 1, wherein the internal clock signal generator comprises:

a phase controller, which outputs ~~an~~ a delayed version of the output signal of the level selector as the internal clock signal, in response to first and second phase control signals;

a feedback unit, which compares a phase of the internal clock signal with a phase of the external clock signal and generates an up/down signal and a mode signal; and

a phase control signal generator, which generates the first and the second phase control signals for controlling a phase of the output signal of the level selector, in response to the mode signal and the up/down signal;

wherein the phase controller includes a delay chain for receiving the output signal of the level selector.

13. (Original) The DLL of claim 12, wherein the delay chain includes differential amplifier type analog delay cells having a small swing width.

14. (Original) The DLL of claim 1, wherein the level selector receives the external clock signal through a repeater circuit.

15. (Currently Amended) A delay-locked loop (DLL) comprising:

a level selector, which receives an external clock signal, and directly outputs the external clock signal, or changes a level of the external clock signal and outputs a changed external clock signal; and

an internal clock signal generator, which receives an output signal of the level selector and the external clock signal, and generates an internal clock signal synchronized to a phase of the output signal of the level selector,

wherein the level selector receives the external clock signal through a repeater circuit.

16. (Original) The DLL of claim 15, wherein the level selector comprises:

a clock buffer unit, which receives the external clock signal and outputs the changed external clock signal;

a first metal line, which directly applies the external clock signal to the internal clock signal generator; and

a second metal line, which applies the external clock signal to the clock buffer unit,

wherein one of the first and the second metal lines is connected and one of the first and the second metal lines is disconnected.

17. (Original) The DLL of claim 16, wherein the clock buffer unit amplifies a level of an input signal to a complementary metal oxide semiconductor (CMOS) level.

18. (Original) The DLL of claim 15, wherein the level selector comprises:

a clock buffer unit, which receives the external clock signal and outputs the changed external clock signal;

a first pad which receives the external clock signal;

a second pad which receives the external clock signal;

a third pad, which corresponds to the first pad and is connected to the internal clock signal generator; and

a fourth pad, which corresponds to the second pad and is connected to the clock buffer unit;

wherein the first pad and the third pad is connected by a bonding wire or the second pad and the fourth pad is connected by a bonding wire.

19. (Original) The DLL of claim 18, wherein the clock buffer unit amplifies a level of an input signal to a CMOS level.

20. (Original) The DLL of claim 18, wherein the first and the third pads are connected with a fuse with the second and fourth pads disconnected, or the second and the fourth pads are connected with a fuse with the first and third pads disconnected.

21. (Original) The DLL of claim 20, wherein the fuse is a laser fuse.

22. (Original) The DLL of claim 15, wherein the external clock signal has a Transistor-Transistor Logic (TTL) level.

23. (Currently Amended) The DLL of claim 15, wherein the internal clock signal generator comprises:

a phase controller, which outputs ~~an~~ a delayed version of the output signal of the level selector as the internal clock signal, in response to first and second phase control signals;

a feedback unit, which compares a phase of the internal clock signal with a phase of the external clock signal and generates an up/down signal and a mode signal; and

a phase control signal generator, which generates first and second control signals for controlling a phase of ~~an~~ the output signal of the level selector, in response to the mode signal and the up/down signal,

wherein the phase controller includes a delay chain for receiving ~~an~~ the output signal of the level selector.

24. (Original) The DLL of claim 23, wherein the delay chain includes differential amplifier type analog delay cells having a small swing width.

25-29. (Canceled)